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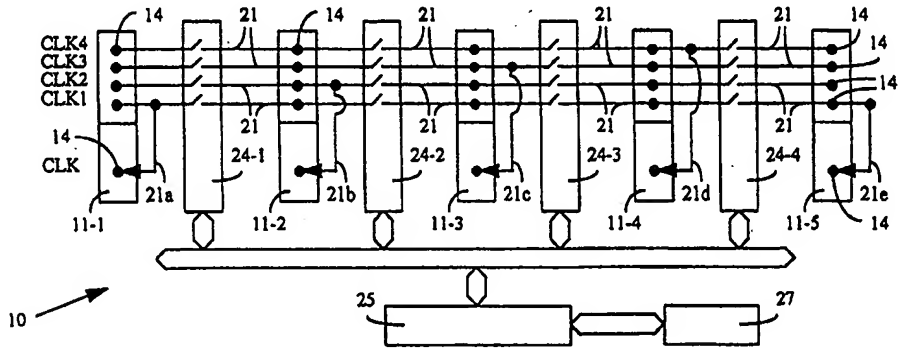
(54) Title: INTERCONNECTION CIRCUIT FOR ELECTRONIC MODULES



(57) Abstract

This invention relates to a circuit (10) for interconnecting electronic modules in a data and/or commands channel (bus) segment. The circuit (10) comprises a plurality of connectors (11–1÷11–5) designed to accommodate electronic modules of the same type or different types and a plurality of Pins (14) associated with the connectors and interconnected through a plurality of electric connections (21). The electric connections (21) between the Pins (14) of the connectors (11–1÷11–5) are controlled by electronic switches (24–1÷24–4) in such a way that a plurality of sub–segments, each comprising a subset of the connectors (11–1÷11–5), is obtained from a bus segment. Moreover the connections (21) are made in such a way that it is possible to accommodate the different types of electronic modules, for example system modules and peripheral modules, in any position of the bus segment.

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INTERCONNECTION CIRCUIT FOR ELECTRONIC MODULES

Technical Field

This invention relates to an interconnection circuit for electronic modules comprising a support having a plurality of electric connection points and suitable for constituting a data and/or commands channel (bus) segment, a plurality of connectors connected to the connection points and each suitable for accommodating a corresponding electronic module, and interconnection means for connecting the connection points to each other.

The invention relates more particularly to an interconnection circuit made in compliance with the PCI (Peripheral Component Interconnect bus) data and commands channel specifications called CompactPCI™, as defined by the manufacturers' committee called PICMG (PCI Industrial Computers Manufacturing Group).

Background Art

Interconnection circuits are known, in particular wired circuits for interconnecting electronic modules in systems having a data and command channel or bus architecture.

Systems with a bus architecture generally comprise a wiring board and a plurality of connectors or slots, soldered on the board, into which the various electronic modules are inserted.

Known in particular from the CompactPCI™ PICMG 2.0 R2.0 specifications are the dimensions and the architecture of the wiring circuits for interconnecting numerous CompactPCI™ electronic modules.

According to these specifications, the general principles of which may however be extended, with the exception of a few details, to all the systems with bus architecture, a CompactPCI™ system consists of one or more segments for the transfer of data and commands (bus segments) each of which comprises a wiring board capable of housing up to a maximum

of 8 slots for accommodating a like number of electronic modules.

In particular, one slot in a predefined position in each of these segments, known as the System Slot, is dedicated to accommodating a system module, or System Slot board, whereas the other slots (Peripheral Slots) are dedicated to accommodating peripheral modules.

Accordingly a bus segment in general, and a CompactPCI™ one in particular, with for instance 8 slots, may accommodate one system module in a predefined position and up to a maximum of 7 peripheral modules in as many Peripheral Slots.

In a system with bus architecture in general, or in a CompactPCI™ segment in particular, the system module and relative slot, in a fixed position, are arranged to exchange through the wiring board, all the reference signals, also called point-to-point signals, such as for example the clock signal, the interrupt signals, etc., with the peripheral modules. Accordingly the wiring board of a bus architecture system will contain not only the bus type connections, but also the so-called point-to-point connections, for interconnecting the "System Slot" with the "Peripheral Slots".

A first technical problem shared by all the bus architecture systems is that once a bus segment comprising a given number of slots has been defined, it is not possible to reconfigure the segment thus set up into numerous segments, each having a subset of the slots of the starting segment.

It may happen therefore that, if a single peripheral module saturates the bus from and to the system module, the other "Peripheral Slots" present in the bus segment are unusable.

A further problem that may arise in a system having a bus architecture, and in a CompactPCI™ segment in particular, is that, in the event of a system module failure, only the replacement of this module in the "System

Slot" allows system functionality to be restored, since none of the "Peripheral Slots" may be used to accommodate a system module.

Disclosure of the Invention

The object of this invention is to produce a circuit for interconnecting systems having a bus architecture that does not have the problems illustrated above.

In particular, the object of this invention is to produce a bus segment dynamically reconfigurable into numerous bus segments or sub-segments, each comprising a subset of the total number of slots included in the bus segment itself.

This technical problem is solved by the interconnection circuit for electronic modules characterized in that electronic switching means are provided for selectively interrupting the connection made by the interconnection means and selectively obtaining from the bus segment a plurality of sub-segments, each comprising a subset of the connectors.

In accordance with a further characteristic of this invention, the interconnection or wiring circuit according to the invention allows the system module and the peripheral modules to be accommodated in any slot, so that the restriction of having a single position available for the system module is eliminated.

Brief Description of Drawings

These and other characteristics of the present invention will become apparent in the course of the following description, provided as a non-exhaustive example of a preferred embodiment, taken in conjunction with the accompanying drawings, where:

Fig. 1 is a wiring board according to the CompactPCI™ specifications;

Fig. 2 is a logic diagram of the connections for clock signals (CLK#) according to the invention;

Fig. 3 is a logic diagram of the connections for interrupt signals (INTA÷D) according to the invention; and

Fig. 4 is a logic diagram of the connections for connection request signals (REQ#) and request acknowledgement signals (GNT#) according to the invention.

Best mode for Carrying Out the Invention

With reference to Fig. 1 a circuit for interconnecting electronic modules or bus segment 10 comprises a wiring board 12, for example made in accordance with the CompactPCI™ specifications, and a plurality of slots, for example from 11-1 to 11-8, located at predefined distances from each other and each suitable for accommodating an electronic module.

The first slot 11-1 is dedicated, for example, to accommodating a system module and is marked with a first type of reference 11a, whereas the other slots, from 11-2 to 11-8 are suitable for accommodating peripheral modules and are marked with a second type of reference 11b.

The wiring board 12 also comprises, associated with each slot, from 11-1 to 11-8, a plurality of connection points or Pins 14, suitable for exchanging electric signals between the wiring board 12 and the electronic modules, and a plurality of electric connections suitable for interconnecting the Pins 14 of the slots 11-1÷11-8.

In order to be able to place the system module in any slot 11-1÷11-8 of the bus segment 10, the electric connections between the Pins for the clock (CLK#), interrupt (INTA÷D), connection request (REQ#), request acknowledge (GNT#) and IDSEL signals, as defined by the CompactPCI™ specifications, must be made appropriately on the wiring board 12.

In particular, on a wiring board 12 made in accordance with this invention and having 5 slots (Fig.2), from 11-1 to 11-5, the connections 21 for the signals CLK# are made in the following way.

The PIN for the signal CLK1 of the first slot 11-1 is connected to the PIN for the signal CLK1 of the slot 11-2 and so on, to the last slot 11-5.

Similar type bus connections 21 are made for the Pins of the signals CLK2, CLK3 and CLK4.

In addition, in the first slot 11-1, the PIN for the signal CLK1 is connected to the PIN for the signal CLK with a first connection 21a; in the second slot 11-2, the PIN for the signal CLK2 is connected to the PIN for the signal CLK with a second connection 21b; in the third slot 11-3, the PIN for the signal CLK3 is connected to the PIN for the signal CLK with a third connection 21c; in the fourth slot 11-4, the PIN for the signal CLK4 is connected to the PIN for the signal CLK with a fourth connection 21d; in the fifth slot 11-5, a fifth connection 21e is made, similar for example to the one made in the first slot 11-1, and so on, where there are more than 5 slots present.

Naturally the alternation of the latter type of connections, from 21a to 21e may be made in any order without altering the spirit of the invention.

The connections 22 (Fig.3) for the signals INTA÷D are made in the following way.

The PIN for the signal INTD of the first slot 11-1 is connected to the PIN for the signal INTC of the slot 11-2, and so on in sequence until the PIN for the signal INTA of the fourth slot 11-4 is connected to the PIN for the signal INTD of the last slot 11-5.

The PIN for the signal INTC of the first slot 11-1 is connected to the PIN for the signal INTB of the slot 11-2 and so on in sequence until the PIN for the signal INTD of the fourth slot 11-4 is connected to the PIN for the signal INTC of the last slot 11-5.

The PIN for the signal INTB of the first slot 11-1 is connected to the PIN for the signal INTA of the slot 11-2 and so on in sequence, in the same way as already described for the signals INTA and INTB.

The PIN for the signal INTA of the first slot 11-1 is connected to the PIN for the signal INTD of the slot 11-2

and so on in sequence, in the same way as already described for the signals INTA and INTB.

The connections 23 (Fig.4) for the signals REQ# and GNT#, described here together for simplicity's sake and confined to the signals REQ0-4 and GNT0-4 only, are made in the following way.

The Pins for the signals REQ0 and GNT0 of the first slot 11-1 are connected to the Pins for the signals REQ4 and GNT4 of the slot 11-2, the latter to the Pins for the signals REQ3 and GNT3 of the slot 11-3, and so on in sequence until the Pins for the signals REQ2 and GNT2 of the slot 11-4 are connected to the Pins REQ1 and GNT1 of the last slot 11-5.

Similarly, the Pins for the signals REQ1 and GNT1 of the first slot 11-1 are connected to the Pins for the signals REQ0 and GNT0 of the slot 11-2, the latter to the Pins for the signals REQ4 and GNT4 of the slot 11-3, and so on in sequence, until the Pins for the signals REQ3 and GNT3 of the slot 11-4 are connected to the Pins REQ2 and GNT2 of the last slot 11-5.

Similarly, the connections of the Pins for the signals REQ2 and GNT2, REQ3 and GNT3, REQ4 and GNT4 of the slot 11-1 are made to the other slots 11-2÷11-5.

Finally, not illustrated in Figures, the PIN for the signal IDSEL of the first slot 11-1 is connected, in the same way as defined by the CompactPCI™ specifications for the Peripheral Slots, to the PIN for the signal AD25, in such a way that even a peripheral module may be accommodated in the first slot 11-1.

In order to be able to dynamically reconfigure the bus segment 10 into numerous bus segments or sub-segments, in accordance with this invention, it must be possible to suitably control all of the connections, both the bus type connections, not depicted in the figures, and the point-to-point connections 21, 22, 23 (Fig.2, Fig.3 and Fig.4)

between the Pins for the signals CLK#, INTA÷D and REQ# GNT#.

In particular, located between the slots 12-1 and 12-2, 12-2 and 12-3, 12-3 and 12-4 and 12-4 and 12-5 respectively, the bus segment 10, in accordance with this invention, comprises a plurality of electronic switches 24-1, 24-2, 24-3 and 24-4 suitable for simultaneously interrupting all the connections, whether bus or point-to-point type, between one slot and another.

The interconnection circuit 10 also comprises a control unit 25 connected to the switches 24-1÷24-4 and suitable both for memorising information and programs developed in the stage of designing the circuit 10 itself and also for selectively commanding one or more of the switches 24-1÷24-4 to interrupt or restore the connections between the slots.

Finally the interconnection circuit 10 comprises a known type interface device 27, connected to the control unit 25, for receiving data and commands from external devices.

The electronic switches 24-1÷24-4 could, for example, be the high speed components, model QS32384 made by the Quality Semiconductor company.

The control unit 25 could, for example, be the microprocessor model 80C51 produced by the INTEL company.

Operation of the interconnection circuit 10 described up to this point is as follows.

In the event that the System Slot is slot 11-1, the signals CLK#, INTA÷D and REQ# GNT# are handled in the same way as established by the CompactPCI™ specifications.

If the System Slot is assigned to a different slot, for example to slot 11-3, once again the signals CLK#, INTA÷D, REQ# GNT# and IDSEL are handled in the same way as established by the CompactPCI™ specifications.

In fact the signal CLK#, in accordance with the specifications, is generated by the system module on the pins for the signals CLK1, CLK2, CLK3 and CLK4 and is

transmitted to the Peripheral Slots 11-1, 11-2, 11-4 and 11-5, from where it is sent to the PIN for the signal CLK of each of the slots by means of the connections 21a÷21e.

Similarly the signal INTA which is generated, in accordance with the CompactPCI™ specifications, by each peripheral module and transmitted to the system module, will be received in the System Slot 11-3 on the pins for INTD and INTC as regards the slots 11-4 and 11-5 respectively and on the pins for INTD and INTC respectively as regards the slots 11-2 and 11-1.

In the same way, the connection request signals REQ# generated by each peripheral module on the PIN for the signal REQ0 will be received by the system module on the PIN for REQ1 for the slot 11-4, on the PIN for REQ2 for the slot 11-5, on the PIN for REQ3 for the slot 11-2 and on the PIN for REQ4 for the slot 11-1, thus maintaining correspondence with the signals INT# already described.

Moreover, the signal IDSEL is handled in such a way in the first slot 11-1 that a peripheral module may be inserted therein.

Therefore all the point-to-point signals described, whatever the position of the system module, will be handled and the relative position of each peripheral module with respect to the system module may easily be reconstructed through suitable tables memorised, for example, in the control circuit 25.

Additionally, in accordance with one of the characteristics of this invention, by accommodating a system module in the slot 11-1 and one in the slot 11-3 and by commanding, by means of the control unit 25, the opening for example of the electronic switch 24-2, from a bus segment 10 having 5 slots, it is possible to obtain two bus segments, the first having two slots, 11-1 and 11-2, and the second three slots, 11-3, 11-4 and 11-5.

Naturally, through the control and activation of the electronic switches, a plurality of segments may be obtained from a single bus segment.

It is also clear that the interconnection circuit 10 according to this invention may be used to produce redundant systems.

To this end, by placing for example a first system module in the slot 11-1 and a second system module in the slot 11-5, it is possible to operate the entire bus segment either under the control of the first system module or, alternatively, under the control of the second, by suitably activating the electronic switches 24-1 and 24-4.

In accordance with a second embodiment, not illustrated in Fig.2, the electronic switches 24-1÷24-4 of the clock signals, CLK1÷CLK4, are controlled selectively and independently, in order to avoid problems of attenuation on the connections 21a-21e on account of reflections on the bus type connections 21.

In accordance with a third embodiment, not illustrated in Fig.2 and as an alternative to the above example, the electronic switches 24-1÷24-4 of the clock signals, CLK1÷CLK4, are switched upon loads having an impedance corresponding to the characteristic impedance of the bus type connections 21.

In accordance with a fourth embodiment, not illustrated in Fig.2 and as an alternative to the above examples, the signal CLK is generated, not by the connections 21a÷21e, but by independent connections coming from the control circuit 25 and controlled by the system module of each bus segment.

In accordance with yet another variant, the control unit 25 of the interconnection circuit 10 (Fig.2, Fig.3 and Fig.4) may be produced by using the logic circuitry present on a system module and by programming it appropriately. In this case, it is not necessary for a control unit or an interface device to be present on the interconnection

circuit 10. Naturally, in an embodiment of this kind, the system module accordingly produced will act as a supervisor of the interconnection circuit 10 as a whole.

Though the description refers to the CompactPCI™ specifications, it is clear that the embodiment described may easily be extended to interconnection circuits of any type, with any number of slots, with one or more slots assigned for system modules.

Changes may be made to the dimensions, shapes, materials, components, circuit elements, connections and contacts, as also to the details of the circuitry, method of construction and method of operation without exiting from the scope of the invention.

CLAIMS

1. Interconnection circuit for electronic modules comprising

- a support (12) having a plurality of electric connection points (14) and suitable for constituting a data and/or commands channel (bus) segment,

- a plurality of connectors (11-1÷11-5) connected to said connection points (14) and each suitable for accommodating a corresponding electronic module, and

- interconnection means (21÷23) for connecting said connection points (14) to each other; characterized in that

- electronic switching means (24-1÷24-4) are provided for selectively interrupting the connection made by said interconnection means (21÷23) and selectively obtaining from said bus segment a plurality of sub-segments, each comprising a subset of said connectors (11-1÷11-5).

2. Interconnection circuit according to claim 1 characterized in that

- control means (25) are provided for selectively controlling said electronic switching means (24-1÷24-4).

3. Interconnection circuit for electronic modules, both system and peripheral type, suitable for exchanging point-to-point type signals (CLK#, INT#, REQ#, GNT#), comprising

- a support (12) having a plurality of electric connection points (14),

- a plurality of connectors (11-1÷11-5) connected to said connection points (14) and suitable for accommodating at least one electronic system module and a plurality of electronic peripheral modules, and

- interconnection means (21÷23) connecting given connection points together in order to permit the exchange of said point-to-point type signals (CLK#, INT#, REQ#, GNT#); characterized in that

- said interconnection means (21÷23) are arranged in such a way that said system module is connected to all the peripheral modules in order to permit the exchange of said point-to-point type signals (CLK#, INT#, REQ#, GNT#) between said system module and each of said peripheral modules, regardless of the position of the connector (11-1÷11-5) wherein said system module is accommodated.

4. Interconnection circuit according to claim 3 characterized in that

- said point-to-point type signals (CLK#, INT#, REQ#, GNT#) comprise timing or clock signals, interrupt signals, exchange request signals and signals acknowledging said exchange request signals.

5. Interconnection circuit according to claim 3 wherein said support (12) with said plurality of connection points (14) is suitable for constituting a data and/or commands channel (bus) segment, characterized in that

- electronic switching means (24-1÷24-4) are provided for selectively interrupting the connection made by said interconnection means (21÷23) and selectively obtaining from said bus segment a plurality of sub-segments, each comprising a subset of said connectors (11-1÷11-5).

6. Interconnection circuit according to claim 5 characterized in that

- control means (25) are provided for selectively controlling said electronic switching means (24-1÷24-4).

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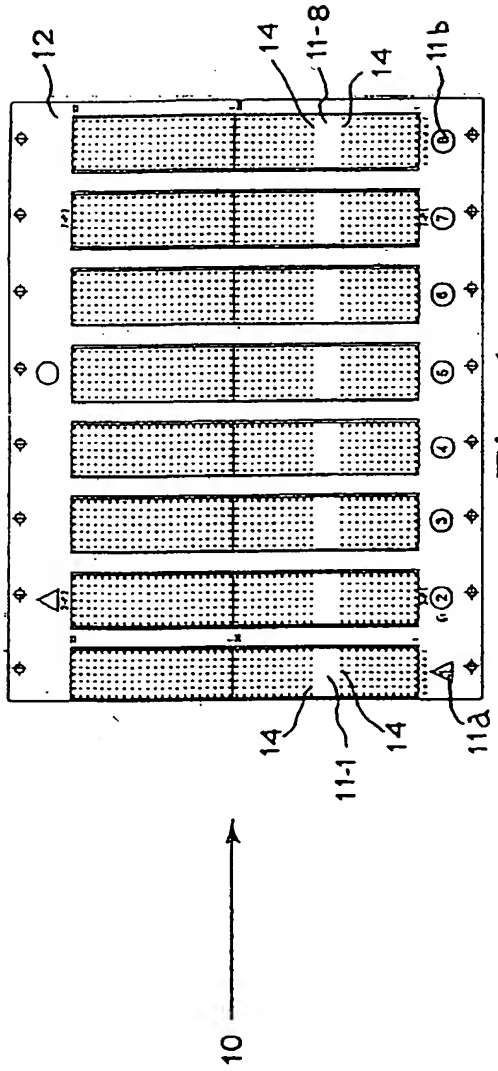
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11a
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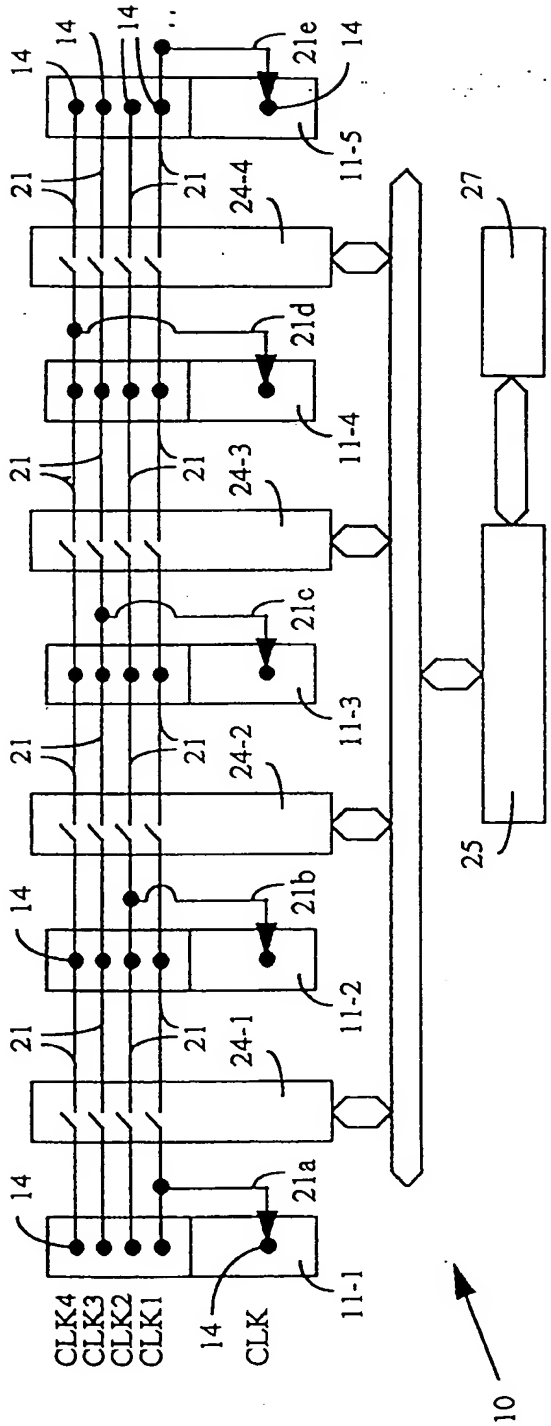
Fig. 1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21
24-4
21d
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24-3
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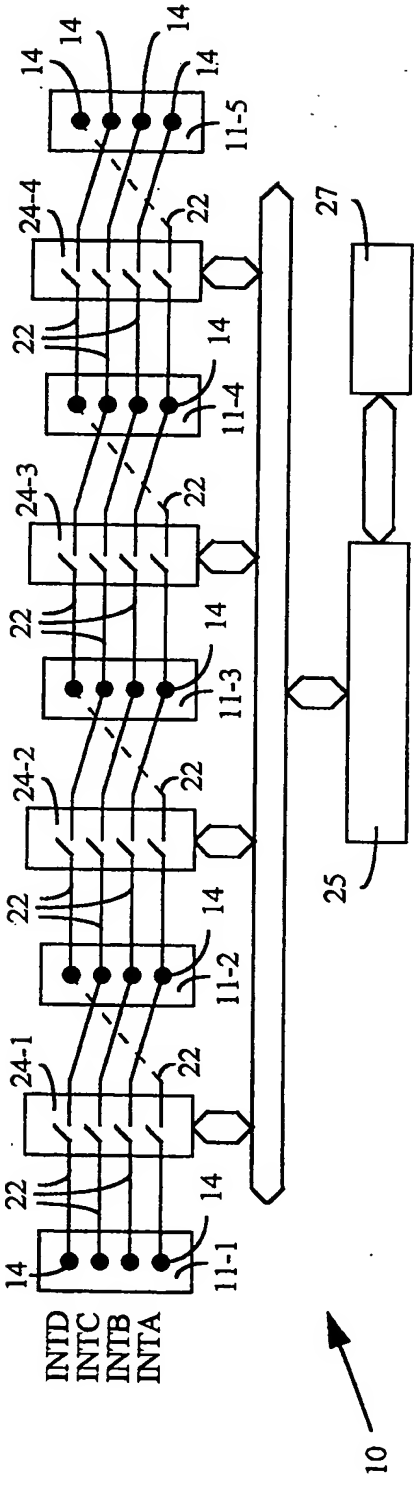
CLK1
CLK
27
25
10

Fig. 2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INTB
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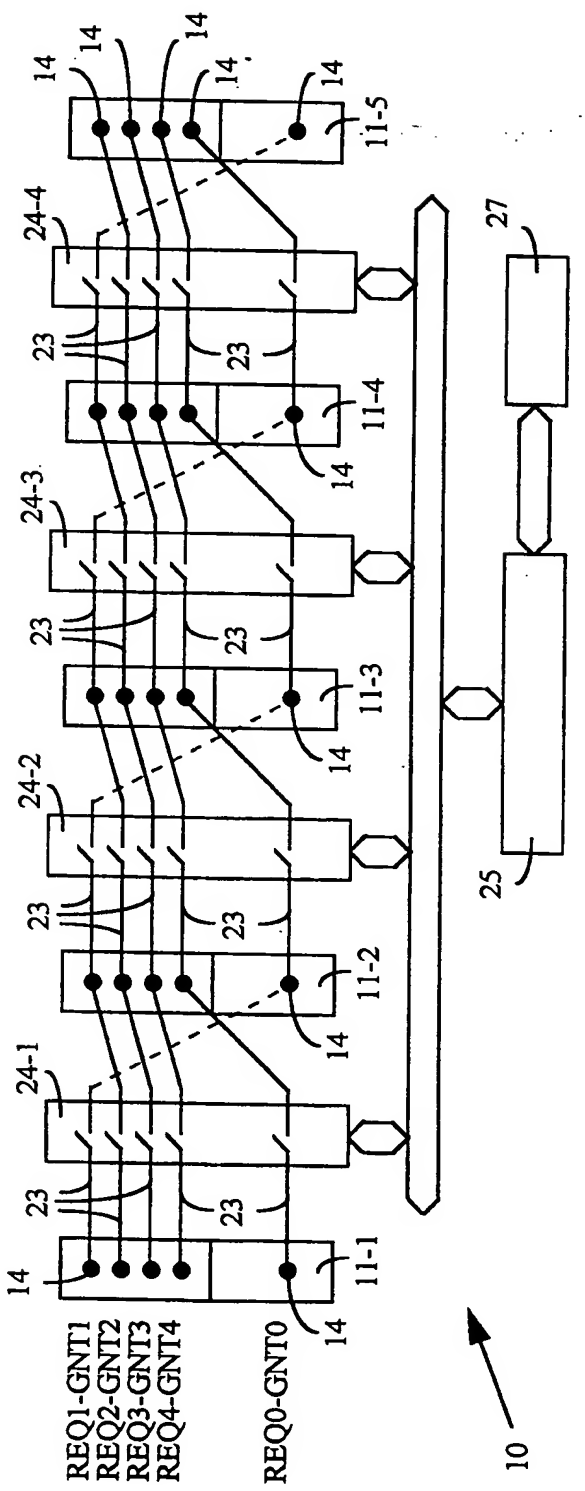
27
14
22

Fig. 3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REQ3-GNT3
REQ4-GNT4
REQ0-GNT0
10
11-1
11-2
11-3
11-4
11-5
24-1
24-2
24-3
24-4
25
27
14
23

Fig. 4

INTERNATIONAL SEARCH REPORT

Inter ıal Application No
PCT/IT 98/00238

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 93 15464 A (KELLY RALPH HAROLD) 5 August 1993	1-4
A	see page 1, paragraph 2 see page 3, paragraph 3 - page 5, paragraph 1 see page 11, paragraph 3 - page 13, paragraph 1 see page 14, paragraph 2 - page 15, paragraph 1 see abstract; figures 2,4	5,6
A	US 5 122 691 A (BALAKRISHNAN BALU) 16 June 1992 see column 1, line 21 - line 61 see column 2, line 61 - column 3, line 32 see column 5, line 13 - column 6, line 35 see abstract; figures 3-5	1-6

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[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 December 1998	23/12/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nguyen Xuan Hiep, C

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 583 998 A (BOWMAN DAVID A) 10 December 1996 see column 1, line 33 - line 56 see column 2, line 59 - column 3, line 6 see column 5, line 49 - column 6, line 59 see abstract; figures 2-5	1-6

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